ABSTRACT

A process for forming an integrated circuit calls for the provision of at least one matrix of non-volatile memory cells including an intermediate dielectric multilayer comprising a lower silicon oxide layer, an intermediate silicon nitride layer and an upper silicon oxide layer. The process calls for the simultaneous provision in zones peripheral to the memory cells of at least one first and one second transistor type each having a gate dielectric of a first and a second thickness respectively. After formation of the floating gate of the cells with a gate oxide layer and a polycrystalline silicon layer and the formation of the lower silicon oxide layer and of the intermediate silicon nitride layer, the process in accordance with the present invention includes removal of said layers from the zones peripheral to the matrix, and formation of a first silicon oxide layer over the substrate in the areas of both types of transistor. The process further includes removal of the preceding layer from areas assigned only to the transistors of the second type; deposition of said upper silicon oxide layer over the memory cells, over the first silicon oxide layer in the areas of the transistors of the first type and over the substrate in the areas of the transistors of the second type; and formation of a second silicon oxide layer in the areas of both types of peripheral transistors.